**Face-To-Face Student/Supervisor Meeting Record**

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| **Project Title:** | Design and Implementation of a Multi-core Processor using FPGA | **Photo:** |  |
| **Student Name:** | Matteo Bovino | **Student ID:** | 8671055 |
| **Supervisor:** | Dr Server Kasap | **Student UID:** |  |
| **Supervisor UID:** |  | **Department:** | AAEEE |
| **Course Code:** | Electrical and Electronic Engineering | **Module Code:** | 306AAE |
| **Date Today:** | 02/04/2021 | **Time:** | 02:00 PM |

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| **Current Progress and Issues:** | |
| *After multiple unsuccessful attempts to synthesize the SystemVerilog code, I have decided to forgo the hardware implementation of the design itself. Although the root cause of these issues is known, fixing them would require an extensive period of time, which would then impact the presentation and dissertation. Due to the new regulations governing the project, we both agreed to prioritize the reports and to start writing the first drafts immediately. This is the last phase of the project and the most crucial one, allowing more time for it is undoubtedly the best decision.* | |
| **Agreed Key Action Points:** | |
| *In this meeting we also agreed on some key points regarding the future development of the project. We first set a virtual deadline for the upcoming meeting, in which I’ll have to produce an initial draft of the report. We also discussed the amount of time that should be invested in order to write clear and up to standard documents. Finally, given the lack of clarity surrounding the deadlines for the project, I was advised to email the module leader asking for specific dates in order to have a better time plan.* | |
| **Date and Time of next meeting:** | 02:00 PM 16/04/2021 |

*Signatures of those present:*

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| **Supervisor:** |  |
| **Student: Matteo Bovino** |  |